IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Sun J Lin
Frederic Reblewski	Art Unit: 2825
Application No.: 10/043,964	Confirmation No.: 6410
Filed: Jan. 10, 2002	Customer No.: 25943
For: CROSSBAR DEVICE WITH REDUCED PARASITIC CAPACITIVE LOADING AND USAGE OF CROSSBAR DEVICES IN RECONFIGURABLE CIRCUITS	

Mail Stop Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.323

Dear Commissioner:

Upon review of the above-referenced Letters Patent, Applicant noted errors that are the mistake of the U.S. Patent and Trademark Office.

Please correct the following:

at col. 5, line 24, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 5, line 44, "raise a voltage raised by" should read --raise a voltage by--

at col. 5, line 53, "wherein each the" should read --wherein each of the--

at col. 5, line 54, "pass transistors coupled" should read --pass transistor coupled--

at col. 5, line 58, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 5, line 65, "wherein each the" should read --wherein each of the--

at col. 6, line 3, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 6, line 7, "coupled a pass" should read --coupled to a pass--

at col. 6, line 13, "reconfigurable logic circuit" should read --reconfigurable circuit--

at col. 6, line 35, "wherein each the" should read --wherein each of the--

at col. 6, line 40, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 6, line 53, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--

at col. 8, line 2, "some know logic" should read --some known logic--

Applicant believes no fee is required for these corrections. It is respectfully requested that a Certificate of Correction be issued.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: August 27, 2009

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,874,136

APPLICATION NO.: 10/043,964

ISSUE DATE : 03-29-2005

INVENTOR(S) : Frederic Reblewski

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 5, line 24, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--.
Column 5, line 44, "raise a voltage raised by" should read --raise a voltage by--.
Column 5, line 53, "wherein each the" should read --wherein each of the--.
Column 5, line 54, "pass transistors coupled" should read --pass transistor coupled--.
Column 5, line 58, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--.
Column 5, line 65, "wherein each the" should read --wherein each of the--.
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Column 6, line 13, "reconfigurable logic circuit" should read --reconfigurable circuit--.
Column 6, line 35, "wherein each the" should read --wherein each of the--.
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Column 6, line 53, "transistor; where" should read --transistor and wherein a gate of the first pass transistor is coupled to a first signal and a gate of the second pass transistor is coupled to a second signal; where--.
Column 8, line 2, "some know logic" should read --some known logic--.

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